66-16AI32SSC

32-Channel, Differential, 16-Bit Simultaneous Sampling; PMC Analog Input Board

With 200 KSPS Sample Rate per Channel and 66 MHz PCI Support

Available in PMC, PCI, cPCI and PC104-*Plus* and PCI Express form factors as:

PMC66-16AI32SSC:	**PMC**, Single-width
PCI66-16AI32SSC:	**PCI**, short length
cPCI66-16AI32SSC:	**cPCI,** 3U
PC104P66-16AI32SSC:	**PC104-*Plus***
PCIe66-16AI32SSC:	**PCI Express**
PCIe10466-16AI32SSC:	**PCIe, one-lane on PC/104 form factor**

See Ordering Information for details.
Call for availability of other form factors, such as XMC, CCPMC, etc.

Features

- **32 Differential analog inputs with dedicated 200KSPS 16-Bit ADC per channel**
- **Sampling rates to 200 KSPS per channel (6.4 MSPS aggregate rate)**
- **Simultaneous sampling of all inputs; minimum data skew**
- **D32; 66MHz, 33MHz PCI compatibility, with universal 5V/3.3V signaling**
- **Input ranges: ±10V, ±5, ±2.5V; software-selectable**
- **Sync and clock I/O support external control and multiboard configurations**
- **Optional *Time Tagging* is available**
- **A *Low-Latency* option provides 32 registers that duplicate the last sample from all A/D converters**
- Increased throughput capacity with local data packing
- Continuous, burst and single-sample clocking modes
- Hardware sync I/O for multiboard operation
- 1 MByte FIFO data buffer; 512 K-Samples in packed-data mode.
- 2-Channel DMA engine
- Sampling controlled by internal rate generator, by software trigger, or externally
- On-Demand internal Autocalibration of all channels
- Single-width PMC form factor

Typical Applications

✓ High-Density Analog Inputs	✓ Industrial Robotics	✓ Acoustic Sensor Arrays
✓ Analog Event Capture	✓ Biometric Signal Analysis	✓ Dynamic Test Systems

Rev: 110614

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Functional Description

The 16-Bit PMC66-16AI32SSC analog input board samples and digitizes up to 32 input channels simultaneously at rates up to 200,000 samples per second for each channel. Each input channel contains a dedicated 16-Bit sampling ADC, and the resulting sampled data is available to the PCI bus through a 1-MByte FIFO buffer. The 32-Bit local data path supports full D32 local-bus data packing. Throughput capacity is further enhanced with 66MHz PCI support. All operational parameters are software configurable.

Inputs can be sampled in groups of 2, 4, 8, 16 or 32 channels; or any contiguous channel group can be selected for sampling. The sample clock can be generated from an internal rate generator, or by software or external hardware. Input ranges are software-selectable as ±10V, ±5V or ±2.5V.

An on-demand autocalibration feature determines offset and gain correction values for each input channel, and applies the corrections subsequently during acquisition. A selftest switching network routes calibration reference signals to each channel through internal selftest switches, and permits board integrity to be verified by the host..

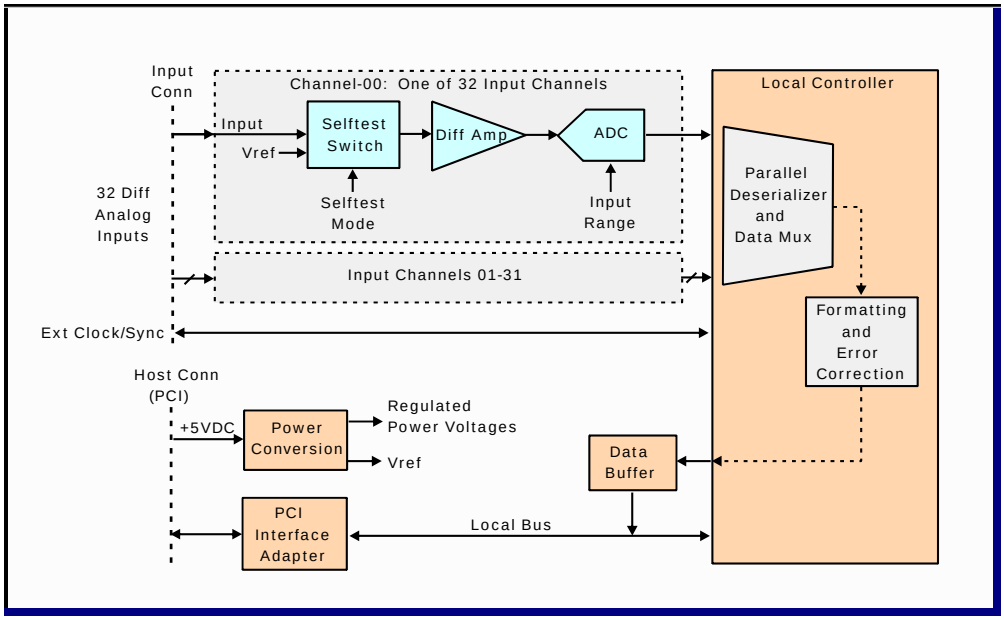

Figure 1. PMC66-16AI32SSC; Functional Organization

This product is functionally compatible with the IEEE PCI local bus specification Revision 2.3, and supports the "plug-n-play" initialization concept. System connections are made at the front panel through an 80-pin I/O connector. Power requirements consist of +5 VDC in compliance with the PCI specification, and operation over the specified temperature range is achieved with conventional convection cooling.

Performance Specifications

At +25 ^{O}C, with specified operating conditions, and with differential processing deselected

Input Characteristics:

Configuration:	32 differential analog input channels. 16-Channel version available.
Voltage Ranges:	Software configurable as ±10V, ±5V or ±2.5V fullscale
Input Impedance:	2.0 Megohms typical, line-line. 1.0 Megohms line-ground..
Bias Current:	100nA maximum.
Common Mode Rejection:	60dB typical, DC-50kHz
Min/Max Input Levels for rated performance:	±11V
Crosstalk Rejection:	85dB typical, DC-50kHz
Input Noise:	0.5 mVRMS; typical, all ranges; 0.01-50kHz
Overvoltage Protection:	Sustained ±15 Volts with power removed; ±30V with power applied.

Transfer Characteristics:

Conversion Resolution:	16 Bits (0.0015 percent of FSR)
Maximum Sample Rate:	200 KSPS per channel
Input Bandwidth (-3dB):	DC to 100 kHz typical..
Channels per Sample:	1-32.

DC Accuracy:
(Maximum composite error after autocalibration)

Range	Zero-Input	Fullscale
±10V	± 1.5mv	± 2.8mv
±5V	± 1.4mv	± 2.5mv
±2.5V	± 0.9mv	± 1.5mv

Integral Nonlinearity:	±0.008 percent of FSR, maximum
Differential Nonlinearity:	±0.004 percent of FSR, maximum

Analog Input Operating Modes and Controls

Input Data Buffer:	FIFO, 1 Megabyte in packed-data mode. An optional 'Low-Latency' array of 32 data registers is available, in addition to the FIFO buffer.
Sample Clock Sources:	Internal rate generator; External Hardware Sync I/O, Software clock. Continuous, Burst and Single-Sample Clocking Modes.
Rate Generator:	Programmable from 0.012-200,000 sample clocks per second. Divides the local master clock to the sample rate. (The standard master clock frequency is 50.000MHz. See ordering information for custom frequencies.)
External TTL Sync, Clock:	Bidirectional TTL lines; available through the I/O connector, or through a 6-pin connector located on the back of the board. Optional Sync-I/O connections in PMC-P1 connector. See ordering options
Input Data Format:	Nonpacked Mode: 16-Bit data word plus single-bit Channel-00 tag. Packed Mode: Lword sync code followed by packed channel data. Even-numbered channels occupy lower word (D00-15), odd channels occupy upper word (D16-31).
Data Format:	Selectable as offset binary or two's complement.
Low Latency:	(Optional) In addition to the FIFO buffer, 32 data registers are directly accessible for minimum latency. (Can not be specified simultaneously with 'Time Tagging').
Time Tagging:	(Optional) Provides 48-Bit 1-microsecond time stamping ('tagging') and windowed burst triggering. (Can not be specified simultaneously with 'Low Latency').

PCI Compatibility:

Conforms to PCI Specification 2.3, with 66MHz/33MHz, D32 and universal signaling (5/3.3 Volt).
Single multifunction interrupt.
DMA transfers as bus master with two DMA channels. Both block and demand modes supported.

Power Requirements

+5VDC ±0.2 VDC at 1.0 Amp maximum, 0.8 Amp typical.

Maximum Power Dissipation: Side-1: 4.0 Watts. Side 2: 1.0 Watt.

Physical Parameters

Height: 13.5 mm (0.53 in)
Depth: 149.0 mm (5.87 in)
Width: 74.0 mm (2.91 in)
Shield: Side-1 is protected by an EMI shield.

Environmental Specifications

Ambient Temperature Range:	Operating: 0 to +65 Degrees Celsius inlet air Storage: -40 to +85 Degrees Celsius
Relative Humidity:	Operating: 0 to 80%, non-condensing Storage: 0 to 95%, non-condensing
Altitude:	Operation to 10,000 ft.
Cooling:	Conventional convection cooling; 150 LFPM

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Ordering Information

Specify the basic product model number followed by an option suffix "-A-B-C-D-E", as indicated below. For extended-temperature operation to +80 Deg-C, add the suffix "I" to the base model number.

For example, model number PMC66-16AI32SSC-32-50M-0-0-0 describes a board with 32 input channels, a standard 50.000MHz master clock frequency, standard Latency, and no custom features.

Basic Model Number	Form Factor
PMC66-16AI32SSC	PMC (Native)
PCI66-16AI32SSC [1]	PCI, short length
cPCI66-16AI32SSC [1]	cPCI, 3U
PCIe66-16AI32SSC [1]	PCI Express
PC104P66-16AI32SSC	PC104-*Plus*
PCIe10466-16AI32SSC [1,2]	PCIe, one-lane on PC/104 form factor

[1] Module installed and tested on an adapter, with mechanical and functional equivalency. Contact factory for availability in native form factors.

[2] PCIe104 supports only the PCIe bus.

Optional Parameter	Value	Specify Option As:
Number of Input Channels	32 Channels	A = 32
	16 Channels	A = 16
Master Clock Frequency:	50.000 MHz	B = 50M
(Standard frequency is 50.000MHz)	(Specify custom frequency; 40-55 MHz)	B = (Custom frequency)M
Custom Feature	No custom features	C = 0
	Time Stamp ('Time Tagging') option [2]	C = TS
Custom Feature No.2	No custom features	D= 0
	Sync signals in PMC connector (PXI)	D= PXI
Data Latency	Standard latency	E = Blank or Zero
	Low-Latency [1,2]	E = LL

[1] The low-latency option provides 32 data registers that duplicate the most recent data written to the buffer.

[2] **The 'Time Stamp' and ' Low-latency' options can not be specified together for a single board.** .

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System Interface Connector

Table 1a. System Input/Output Connector; Standard, Without Time Stamping

ROW-A		ROW-B	
PIN	SIGNAL	PIN	SIGNAL
1	INP00 LO	1	INP17 LO
2	INP00 HI	2	INP17 HI
3	INP01 LO	3	INP18 LO
4	INP01 HI	4	INP18 HI
5	INP02 LO	5	INP19 LO
6	INP02 HI	6	INP19 HI
7	INP03 LO	7	INP20 LO
8	INP03 HI	8	INP20 HI
9	INP04 LO	9	INP21 LO
10	INP04 HI	10	INP21 HI
11	INP05 LO	11	INPUT RTN
12	INP05 HI	12	INPUT RTN
13	INPUT RTN	13	INP22 LO
14	INPUT RTN	14	INP22 HI
15	INP06 LO	15	INP23 LO
16	INP06 HI	16	INP23 HI
17	INP07 LO	17	INP24 LO
18	INP07 HI	18	INP24 HI
19	INP08 LO	19	INP25 LO
20	INP08 HI	20	INP25 HI
21	INP09 LO	21	INP26 LO
22	INP09 HI	22	INP26 HI
23	INP10 LO	23	INPUT RTN
24	INP10 HI	24	INPUT RTN
25	INP11 LO	25	INP27 LO
26	INP11 HI	26	INP27 HI
27	INPUT RTN	27	INP28 LO
28	INPUT RTN	28	INP28 HI
29	INP12 LO	29	INP29 LO
30	INP12 HI	30	INP29 HI
31	INP13 LO	31	INP30 LO
32	INP13 HI	32	INP30 HI
33	INP14 LO	33	INP31 LO
34	INP14 HI	34	INP31 HI
35	INP15 LO	35	INPUT RTN
36	INP15 HI	36	INPUT RTN
37	INP16 LO	37	DIG RTN
38	INP16 HI	38	CLOCK I/O
39	INPUT RTN	39	DIG RTN
40	INPUT RTN	40	SYNC I/O

Table 1b. System Input/Output Connector; With Time Stamping

ROW-A		ROW-B	
PIN	SIGNAL	PIN	SIGNAL
1	INP00 LO	1	INP17 LO
2	INP00 HI	2	INP17 HI
3	INP01 LO	3	INP18 LO
4	INP01 HI	4	INP18 HI
5	INP02 LO	5	INP19 LO
6	INP02 HI	6	INP19 HI
7	INP03 LO	7	INP20 LO
8	INP03 HI	8	INP20 HI
9	INP04 LO	9	INP21 LO
10	INP04 HI	10	INP21 HI
11	INP05 LO	11	INPUT RTN
12	INP05 HI	12	INPUT RTN
13	INPUT RTN	13	INP22 LO
14	INPUT RTN	14	INP22 HI
15	INP06 LO	15	INP23 LO
16	INP06 HI	16	INP23 HI
17	INP07 LO	17	INP24 LO
18	INP07 HI	18	INP24 HI
19	INP08 LO	19	INP25 LO
20	INP08 HI	20	INP25 HI
21	INP09 LO	21	INP26 LO
22	INP09 HI	22	INP26 HI
23	INP10 LO	23	INPUT RTN
24	INP10 HI	24	INPUT RTN
25	INP11 LO	25	INP27 LO
26	INP11 HI	26	INP27 HI
27	INPUT RTN	27	INP28 LO
28	INPUT RTN	28	INP28 HI
29	INP12 LO	29	INP29 LO
30	INP12 HI	30	INP29 HI
31	INP13 LO	31	INP30 LO
32	INP13 HI	32	INP30 HI
33	INP14 LO	33	INP31 LO
34	INP14 HI	34	INP31 HI
35	INP15 LO	35	INPUT RTN
36	INP15 HI	36	REF CLK INP
37	INP16 LO	37	DIG RTN
38	INP16 HI	38	SAMP CLK INP
39	INPUT RTN	39	DIG RTN
40	CLOCK RST INP	40	SAMP CLK OUT

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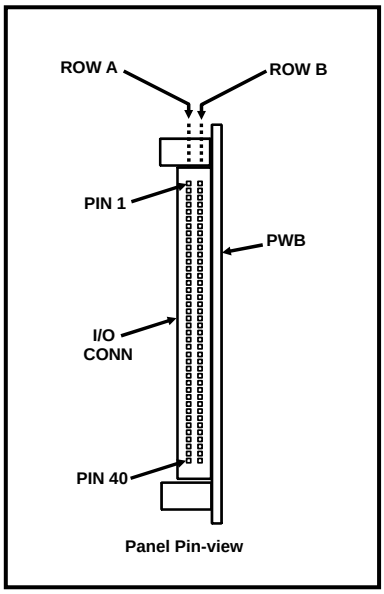

Figure 2. System I/O Connector

System Mating Connector:
Standard 80-pin 0.050" dual-ribbon socket connector:

Robinson Nugent **P50E-080S-TG**
or equivalent.

Table 2. Sync-I/O Connector

SYNC-I/O CONN PIN [1]	PMC CONN PIN [2]	SIGNAL
1	P1-35	DIG RTN
2	P1-41	AUX CLOCK
3	P1-39	DIG RTN
4	P1-42	AUX SYNC
5	P1-44	DIG RTN
6	---	Reserved. Connect to INPUT RTN or leave disconnected.

[1] Recommended Sync-I/O mating cable connector is: Molex# 51146-0600.
[2] SYNC-I/O pins (PXI) in PMC connector P1. DIG RTN is available also on other PMC connector pins.

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